TELEDYNE PHILBRICK

1025/1027/1030 FAST-PRECISION SETTLING FET OPERATIONAL AMPLIFIERS

Teledyne Philbrick Models 1025, 1027, and 1030 operational amplifiers have been designed to provide FAST PRECISION operation. The 1025 is guaranteed to settle to 0.01% of final value in less than 300 nanoseconds while driving 10 V into 200 ohms. The 1030 operates as a unity gain follower and drives a 20 V p-p 5 MHz sine wave into 500 ohm load with minimum distortion. The 1030 provides similar performance as a differential amplifier, or follower with gain.

	GUARANTEED SPECIFICATIONS			
	1027	1027-01	1025	1030
Unity Gain Bandwidth (MHz)	10	10	50	100
Settling Time (μsec) to 0.01%	1	1	0.3	0.5
Slew Rate (V/μsec)	60	60	500	500
Max Sine Power Out (MHz)	0.500	0.500	5.0	5.0
Diff. Input for above specs	yes	yes	no	yes
Output Current (± mA)	20	20	50	20
Offset Voltage vs Temp. (μV/° C)	50	15	50	25
Untrimmed Offset Voltage (mV)	15	15	10	5

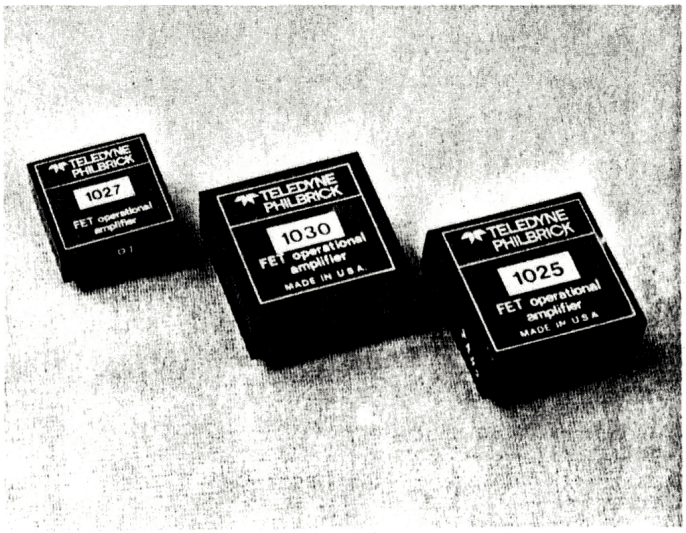
Table 1.

These amplifiers have the open loop gain and dynamic stability (freedom from oscillation) to amplify high speed pulses to a precision of one part in 10,000 and sine waves with less than one percent distortion from dc to 5 MHz.

The differential input capability of the 1027 and 1030 make possible the termination of balanced co-ax lines carrying precision radar signals, wideband RF, IF, or video and the output of high frequency acoustic transducers. A plot of the common mode rejection vs frequency is shown in Figure 1.

Since these devices are true differential input op amps, their dynamic characteristics are inherently the same in both inverting and non-inverting circuits.

The 1027 has guaranteed specifications superior in speed, accuracy, load driving capability and ease of use to the TP monolithic Models 1321 and 1322 at slightly higher cost. In addition, the 1027 shares the FET input characteristics of the 1025 and 1030 making all three amplifiers ideal for fast integrators, sample & holds, peak detectors, buffers, and current-to-voltage converters. The 1025 in particular as an I-to-V makes a fast current DAC into a fast, 50 mA out voltage DAC.



FEATURES

- **250 nanosecond Settling to 0.01% (1025)**
- **True Differential Operation (1027, 1030)**
- **130 MHz Gain Bandwidth Product (1030)**
- **Low Drift (1027-01)**
- **50 mA Output @ ±10 V @ 5 MHz (1025)**

APPLICATIONS

- **Fast Precision**
  - **Buffer**
  - **Sample & Hold**
  - **Video Amp**
  - **Rectifier**
- **Current DAC to Voltage DAC**

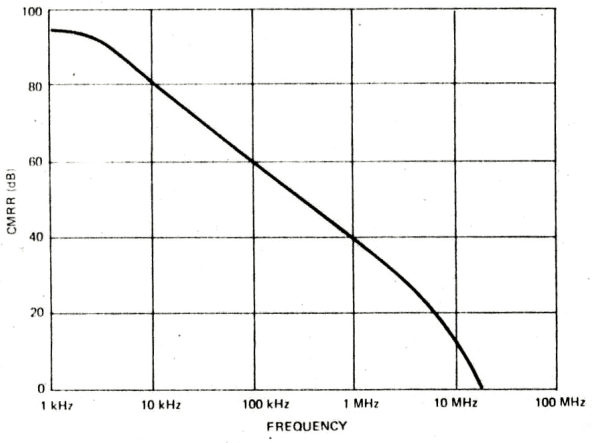


Figure 1. CMRR vs Frequency Model 1030

SETTLING TIME

Settling time is the total time required after application of an input step for a circuit's output to finally settle within a specified error band referred to the steady-state output value. Settling time cannot be predicted from bandwidth and/or slewing rate since a step input, when applied to the amplifier, will cause the output to slew at its maximum rate toward the final value. The output will usually overshoot slightly and "ring" as it settles toward the final value.

Settling time, therefore, includes not only the slew rate, but the ringing time as well. The error band is generally expressed as a percentage of the desired output level, i.e., 0.01% or 1 mV for a 10 volt amplifier.

When observing settling time on an oscilloscope the amplifier may appear to have settled (ringing has ceased) but the value is still outside the error band. It may take a few seconds for this to drift within the error band. This phenomenon is called a "long tail" (see Figure 4) and is often a source of error. The long tails make it virtually impossible to calculate settling time by using slew rate, and ringing characteristics as the sole factors. It should also be realized that knowing the settling time to a given accuracy (say 0.1%) is in no way helpful in extrapolating the settling time to a higher accuracy such as 0.01%.

If settling time cannot be extrapolated, calculated, guessed or ignored, it must be measured. This can be a difficult and misleading task if the proper procedures are not followed precisely.

How to Measure Settling Time

It is not possible to look for 0.1% or 0.01% accuracy directly from an oscilloscope just by looking at the output waveform. At high sensitivity (for resolution), a 10 volt full scale signal will greatly overdrive the scope's input amplifier to the point that its recovery time will probably be much worse than the settling time of interest.

The test circuit shown in Figure 2 is an excellent method for standard settling time measurements. In this circuit, R_{in}, and R_f, are matched to R_{in}' and R_f'. When the AUT has settled to + 0.01% of a 20 volt step in (±2 mV) the settling point (see drawing) will have settled to ± 1mV. An FET with less than 1 pF input capacitance, such as 2N5486, is used as a follower to drive the scope and minimize the capacitance at the settling point. The two 1N914's on the settling point act as limiters and the total capacitance at this point is still less than 3 pF so if $R_f = R_{in}$ = 5 kohms, the lag due to that capacitance can be as low as 8 nanoseconds.

The diode gate and R1, R2 network forms an ideal square wave source for testing since a square wave with significant ripple can cause (unfairly) an amplifier to look bad. Resistors R1 and R2 can be trimmed for desired output.

Measuring settling time to 0.01% requires a clipping amplifier to prevent overloading the oscilloscope's input. The circuit shown in Figure 3 is excellent for this purpose.

For additional information, see the 1430 or 1435 data sheet.

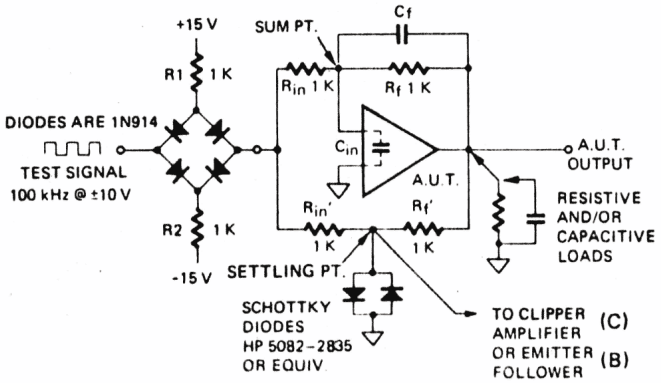


Figure 2. Test Circuit

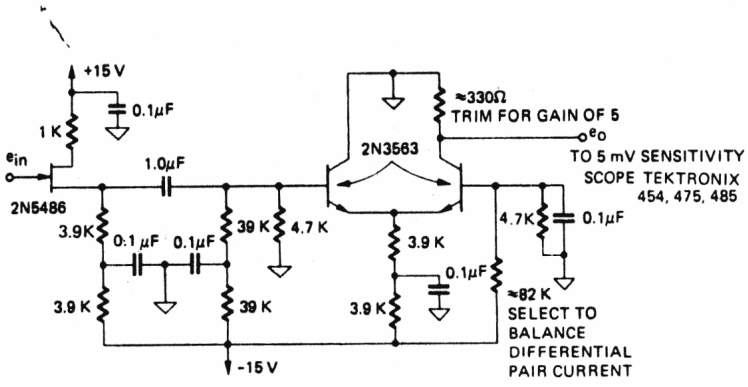


Figure 3. Clipping Amplifier for 0.01% Measurement

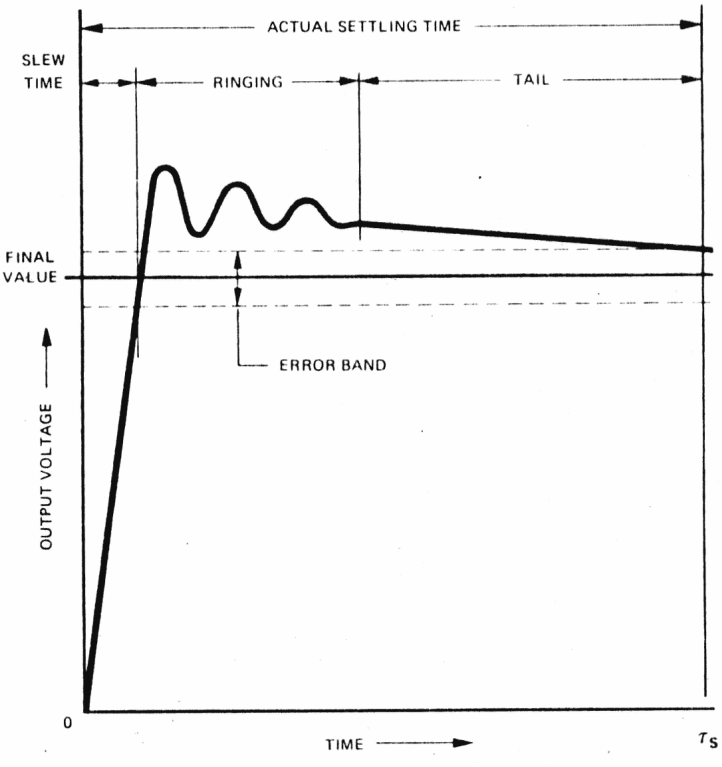


Figure 4. The Composition of Settling Time

APPLICATIONS

In Figure 5, the differential input of the 1030 is combined with the load driving capabilities of two 1025's to provide a 92 Ω balanced line repeater with a gain of 50 from dc to 5 MHz. The 92 Ω input line is matched and terminated (R1) at the 1030 input (A1). The 1030 provides a balanced to single ended gain of 10 and drives the 200 Ω input resistor of A2 (1025). A2 has a gain of 5, providing ±10 V between point A and common. A3 acts as a unity gain inverter, thus providing ∓10 V between point B and common. Thus a 20 V peak to peak balanced, or pushpull, waveform exists between point A and B which drives the 92 Ω output line through 45 Ω matching resistors R2 and R3. When the output line is terminated in 92 Ω, a 10 V p-p signal is impressed on the terminating resistor.

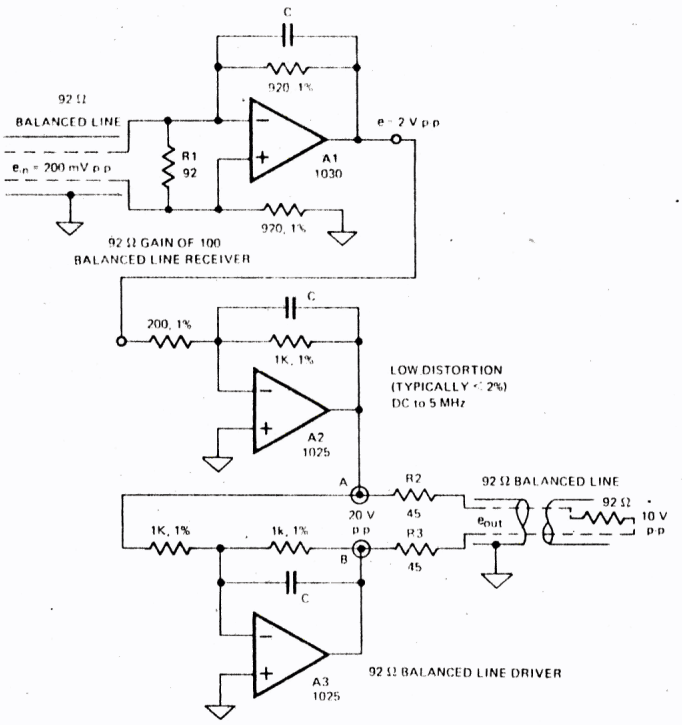


Figure 5. 1030 and 1025 As Balanced Line Repeater

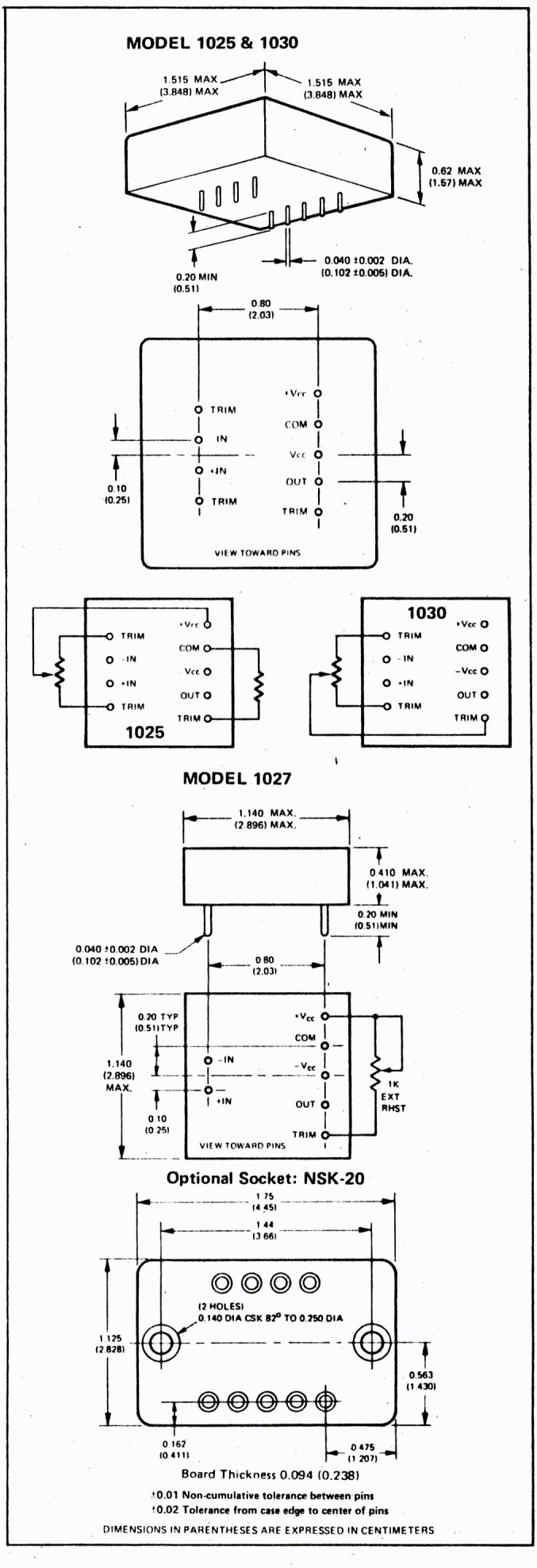
TRIMMING

Most fast-high frequency circuits operate at a gain of less than 100 and often less than 10. The low initial untrimmed offset of these amplifiers (5 mV for the 1030) does not usually require dc trim components. However, each may be externally trimmed as defined below.

1030 The 1030 is zero trimmed with a 100 kΩ potentiometer. If trimming is not required, trim pins are left open.

1027 The 1027 is zero trimmed with a 1 kΩ variable resistor between $+V_{CC}$ and trim pin. If trim is not used, a 499 Ω resistor must be connected between $+V_{CC}$ and trim pin (otherwise E_{OS} may be > 150 mV).

1025 The 1025 is zero trimmed with a 100 kΩ potentiometer. If trimming is not required, trim pins are left open. In addition, a 1 kΩ to 5 kΩ ± 5% settling time trim resistor (provided with unit) must be connected between a trim pin and common. If not used, settling time can double.



SPECIFICATIONS @ +25°C, V_{CC} = ±15 V, unless otherwise indicated

	1025		1027		1030	
	Typical	Guaranteed	Typical	Guaranteed	Typical	Guaranteed
OUTPUT RANGE						
Voltage (peak)	±12 V	±10 V	±12 V	±10 V	±12 V	±10 V
Current	---	±50 mA	±25 mA	±20 mA	---	±20 mA
VOLTAGE GAIN (dc Open Loop)						
Rated Load	106 dB	100 dB	110 dB	100 dB	110 dB	100 dB
FREQUENCY-TIME-RESPONSE						
(Inverting and Non-Inverting) ①						
Small Signal (Gain Bandwidth Product) ②	80 MHz	50 MHz	15 MHz	10 MHz	130 MHz	100 MHz
Max Sine Power Out (3% to 5% distortion)	7 MHz	5 MHz	0.75 MHz	---	7 MHz	5 MHz
Max Peak to Peak Out (Triangle Wave)	10 MHz	---	1.5 MHz	1 MHz	10 MHz	---
Slew Rate	750 V/µsec	500 V/µsec	75 V/µsec	60 V/µsec	850 V/µsec	500 V/µsec
Settling Time (10 V Step Input) ③		④				
to 1% (100 mV)	55 nsec	---	300 nsec	---	70 nsec	---
to 0.1% (10 mV)	90 nsec	---	500 nsec	---	130 nsec	---
to 0.01% (1 mV)	250 nsec	300 nsec	800 nsec	1.0 µsec	300 nsec	500 nsec
Overload Recovery Time (Step Input)	5 µsec	---	1 µsec	---	5 µsec	---
Capacitive Load Without Oscillation ③	500 pF	---	500 pF	---	150 pF	---
INPUT VOLTAGE RANGE						
Common Mode (dc Linear Operation)	±7 V	±4 V	---	±10 V	---	±10 V
Common Mode Fault	±V_{CC} abs. max.	±15 V	±V_{CC} abs. max.	±15 V	±V_{CC} abs. max.	±15 V
Differential (between inputs)	+V_{CC} -(-V_{CC})	30 V	+V_{CC} -(-V_{CC})	30 V	+V_{CC} -(-V_{CC})	30 V
Common Mode Rejection Ratio (DC)	80 dB	---	94 dB	80 dB	94 dB	86 dB
INPUT OFFSET VOLTAGE						
Initial (without external trim) ⑤	±5 mV	±10 mV	2 mV	±15 mV ⑤	±2 mV	±5 mV
Zero Adjustment (optional)	100 kΩ pot	---	1 kΩ rheostat	---	100 kΩ pot	---
Vs. Temperature (Avg. -25°C to +85°C)	24 µV/°C	±50 µV/°C	25 µV/°C	50 µV/°C	15 µV/°C	±25 µV/°C
(1027-01)	---	---	10 µV/°C	15 µV/°C	---	---
Vs. Time (per 24 hours)	±50 µV	---	50 µV	---	50 µV	---
Vs. Power Supply	±100 µV/V	---	300 µV/V	---	±200 µV/V	---
INPUT BIAS CURRENT						
Initial @ 25°C	-10 pA	-20 pA	-20 pA	-50 pA	-10 pA	-20 pA
Vs. Temperature (Avg. -25°C to +85°C)	doubles each 10°C	---	doubles each 10°C	---	doubles each 10°C	---
Vs. Time (per 24 hours)	±2 pA	---	±2 pA	---	±2 pA	---
Vs. Power Supply	±1 pA/V	---	±1 pA/V	---	±1 pA/V	---
Offset (Tracking)	±10 pA	---	±10 pA	---	±10 pA	---
INPUT IMPEDANCE @ dc						
Differential	$10^{11}\Omega \parallel 5$ pF	---	$10^{12}\Omega \parallel 5$ pF	---	$10^{11}\Omega \parallel 5$ pF	---
Common Mode (either Input to Common)	$10^{12}\Omega \parallel 5$ pF	---	$10^{12}\Omega \parallel 5$ pF	---	$10^{12}\Omega \parallel 25$ pF	---
NOISE (Referred to Input)						
Flicker (0.016 to 1.6 Hz)						
Voltage (peak-to-peak)	15 µV	---	5 µV	---	15 µV	---
Current (peak-to-peak)	0.1 pA	---	0.5 pA	---	0.1 pA	---
Midband (1.6 to 160 Hz)						
Voltage (rms)	0.5 µV	---	2 µV	---	0.5 µV	---
Current (rms)	---	---	---	---	0.3 pA	---
Highband (160 Hz to 16 kHz)						
Voltage (rms)	3 µV	---	4 µV	---	3 µV	---
Current (rms)	1 pA	---	---	---	1 pA	---
Broadband (1.6 kHz to 160 kHz)	---	---	10 µV rms	---	---	---
Wideband (8 Hz to 1.6 MHz)	---	---	---	---	12 µV rms	---
POWER REQUIREMENTS						
Voltage Range	±12 to ±18 V	---	---	±12 to ±18 V	±12 to ±18 V	---
Current (Quiescent)	---	±40 mA	---	±12 mA	±17 mA	±20 mA
Current (Full Load)	---	±85 mA	---	±30 mA	±40 mA	---
TEMPERATURE RANGE (Degrees C)						
Operating (Rated)	---	-25 to +85°C	---	-25 to +85°C	---	-25 to +85°C
Operating (Derated)	---	---	---	-40 to +100°C	---	---
Storage	---	-55 to +125°C	---	-55 to +125°C	---	-55 to +125°C

① 1025 may be used non-inverting if CMV < 4 V p-p (7 V p-p typical).
② Measured at 2 MHz for 1025, 10 MHz for 1027, and 1 MHz for 1030.
③ Circuit of Figure 2, 1 K, 1 K inverter, C_f = 15 pF
④ Using supplied settling time trim resistor (2.7 K ± 130 Ω)
⑤ 1027 Initial Offset is ±15 mV with external 499 Ω 1% resistor, ±150 mV if no resistor is used.

The input circuits of these units are protected to ±Vcc. Output circuits are short-circuit protected to ground.

Recommended Power Supply: Teledyne Philbrick Model 2212

TELEDYNE PHILBRICK

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